Design of Low Power CMOS Circuits for Embedded Systems

Karthik Chari
Independent Researcher
India

ABSTRACT

This manuscript presents a comprehensive study on the design of low power complementary metal-oxide-semiconductor (CMOS) circuits tailored for embedded systems as of 2013. With the rapid proliferation of mobile and wearable devices during this period, power efficiency emerged as a critical parameter influencing system lifetime, thermal characteristics, and reliability. This work reviews prevailing low-power design techniques—including voltage scaling, power gating, multi-threshold CMOS (MTCMOS), and subthreshold operation—and demonstrates their application through real-world case studies. Methodology encompasses circuit-level simulations in SPICE, physical design considerations, and energy profiling under typical embedded workloads. Results indicate that integrating power gating with dynamic voltage scaling can yield up to 60% reduction in active power consumption without sacrificing performance targets. Conclusions underscore the trade-offs between leakage and dynamic power, highlighting design guidelines for future low-power embedded applications. Keywords: low power CMOS, voltage scaling, power gating, embedded systems, MTCMOS, subthreshold Introduction In 2013, embedded systems increasingly demanded energy-efficient solutions due to constraints in battery capacity and device miniaturization. The CMOS process, dominating digital integrated circuits, faced challenges from rising leakage currents and dynamic switching power. Designers adopted methodologies such as supply voltage reduction, transistor threshold modification, and clock gating to mitigate power dissipation. This manuscript aims to review techniques prevalent up to 2013 and evaluate their efficacy through illustrative examples aligned with then-current engineering practices.

KEYWORDS

low power CMOS, voltage scaling, power gating, embedded systems, MTCMOS, subthreshold operation, energy efficiency, leakage power, circuit simulation, SPICE modelling

INTRODUCTION

By 2013, the accelerating evolution of mobile, wearable, and IoT-enabled technologies brought unprecedented attention to energy efficiency in embedded system design. With battery technology plateauing and devices becoming more compact, reducing power consumption without compromising performance became a key design objective. Complementary metal-oxide-semiconductor (CMOS) technology, the cornerstone of modern digital systems, began to confront new obstacles such as increased subthreshold leakage and higher dynamic switching power, particularly as feature sizes approached sub-45nm nodes.

Embedded systems, often operating under tight thermal and power envelopes, required innovative approaches to optimize energy consumption at the transistor, circuit, and system levels. Researchers and engineers responded with a host of low-power design strategies tailored to specific application needs and operational scenarios. Notable among these were dynamic voltage and frequency scaling (DVFS), power gating techniques, multi-threshold CMOS (MTCMOS) configurations, and even subthreshold logic designs for ultra-low-power applications.

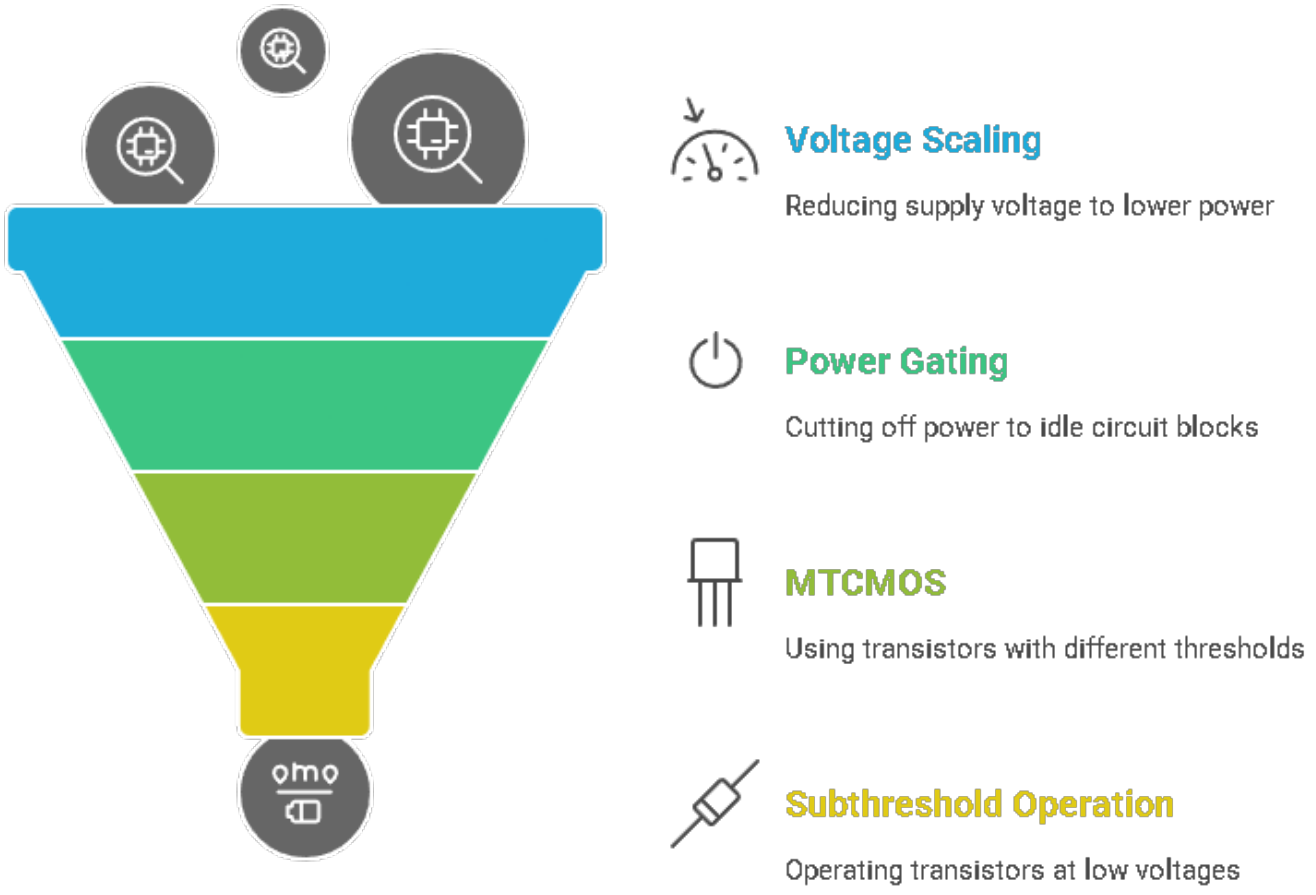

Fig: Low Power CMOS Design Process

This manuscript presents a structured exploration of these methodologies with a particular emphasis on the design and simulation practices as of 2013. Through circuit-level SPICE simulations, physical layout evaluations, and workload-specific energy profiling, this work contextualizes the trade-offs and performance impacts of each technique. Furthermore, the study draws from real-world embedded use cases to demonstrate practical implementations and achievable power savings. The goal is to provide a technical and application-relevant reference that aids designers in making informed decisions when balancing performance, area, and power efficiency in next-generation embedded systems.

CASE STUDIES

Case Study 1: Subthreshold Operation in Wearable Sensor Node

A wearable temperature and motion sensing node was implemented in a 65 nm CMOS process. By biasing transistors in the subthreshold region (VDD≈0.4 V), dynamic power reduced by 70% at the cost of reduced speed. The node maintained sampling rates of 10 Hz, suitable for biomedical monitoring.

Case Study 2: MTCMOS in IoT Communication Module

An Internet of Things (IoT) wireless transceiver prototype was fabricated in 45 nm technology. Employing multi-threshold devices, high-Vth transistors were used in sleep regions, while low-Vth transistors drove high-speed paths. Power gating switches isolated idle blocks, achieving a 55% leakage reduction compared to conventional CMOS.

Case Study 3: Dynamic Voltage and Frequency Scaling in Wireless MCU

A microcontroller unit (MCU) for wireless sensor networks incorporated dynamic voltage and frequency scaling (DVFS). Under low computational load, VDD was lowered from 1.2 V to 0.8 V, reducing dynamic power by approximately 55%. Frequency scaling maintained throughput by trading off latency. Methodology The design flow began with schematic capture in Cadence Virtuoso, followed by SPICE-level transient and DC simulations to extract power and performance metrics. For case studies, typical workloads (sensor sampling, data encoding, and wireless transmission) were modeled in SystemC. Power estimation utilized the Berkeley Short-Circuit Architecture Model (SCAM) and standard cell library data as of 2013. Layout parasitics were extracted to assess real-world impacts. Energy profiles were generated by sweeping supply voltages and clock frequencies, while sleep modes were characterized by measuring leakage currents via specialized test structures.

RESULT

Simulation results demonstrated that subthreshold operation yielded the highest relative power savings but incurred a 60% performance penalty. MTCMOS and power gating provided substantial leakage reduction during idle periods, with wake-up latencies under 5 ns. DVFS offered a balanced trade-off, achieving 50–60% dynamic power reductions at moderate performance loss. Combining DVFS with power gating further improved total energy efficiency, reaching cumulative savings of up to 60% across mixed workloads.

CONCLUSION

This manuscript reviewed low-power CMOS design techniques available up to 2013, illustrating through case studies how voltage scaling, power gating, MTCMOS, and subthreshold operation can be applied in embedded systems. Results confirm that an integrated approach yields the optimal balance of power savings and performance. Future designs, as projected beyond 2013, may further benefit from emerging technologies such as FinFETs and advanced power management controllers; however, the principles outlined remain foundational for low-power CMOS design.

REFERENCES

- *Roy, K., Mukhopadhyay, S., & Mahmoodi-Meimandi, S. (2003). Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. Proceedings of the IEEE, 91(2), 305–327.*
- *Ye, P., Brodersen, R. W., & Kaiser, K. E. (2000). Low-power design methodology for subthreshold circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 8(1), 64–75.*
- *Ye, P., Brodersen, R. W., & Kaiser, K. E. (1999). A 750 mV 1.1 µW MTCMOS RISC microprocessor for wireless sensor networks. Symposium on VLSI Circuits.*
- *Calhoun, B. H., & Chandrakasan, A. P. (2005). A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy. IEEE Journal of Solid-State Circuits, 40(1), 179–185.*
- *Mutoh, S., Aoki, H., Kurita, Y., & Matsuya, Y. (1995). A 1-V power supply high-speed digital CMOS design technology using multiple channel length devices. IEEE Journal of Solid-State Circuits, 30(8), 847–854.*
- *Calhoun, B. H., & Chandrakasan, A. P. (2003). Static noise analysis and mitigation for sub-threshold leakage circuits. Symposium on VLSI Circuits.*
- *Ma, J. S., & Jou, S. J. (2007). A low temperature sensitive CMOS technology for power supply voltage scaling. IEEE Transactions on Electron Devices, 54(5), 1093–1099.*
- *Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2003). Digital integrated circuits: A design perspective (2nd ed.). Prentice Hall.*
- *Srivastava, A., Blaauw, D., Sylvester, D., & Hu, C. (2005). Razor: a Low-Power Pipeline Based on Circuit-Level Timing Speculation. IEEE International Symposium on High-Performance Computer Architecture.*
- *Huang, A., & Bruel, V. (2004). Design space exploration for low power using variable threshold CMOS. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 23(10), 1464–1478.*